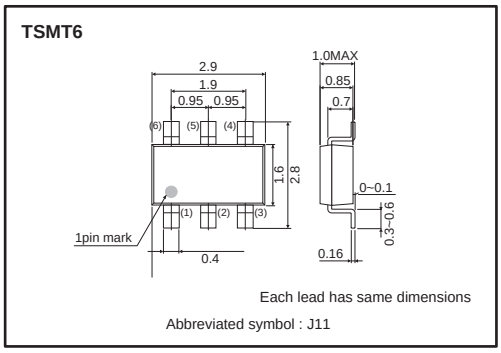
1.5V Drive Pch+Pch MOSFET

QS6J11

●Structure
Silicon P-channel MOSFET

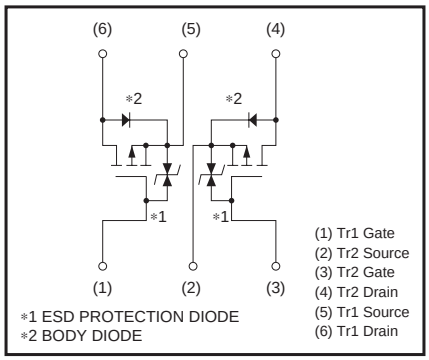
●Features
1) Two Pch MOSFET transistors in a single TSMT6 package.
2) Low on-state resistance with a fast switching.
3) Low voltage drive (1.5V).

●Dimensions (Unit : mm)



●Applications
Switching

●Inner circuit



●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6J11		◯

●Absolute maximum ratings (Ta=25°C)
<It is the same ratings for Tr1 and Tr2>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−12	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	Continuous	I_D	±2	A
	Pulsed	I_{DP} ∗1	±8	A
Source current (Body diode)	Continuous	I_S ∗1	−0.75	A
	Pulsed	I_{SP}	−8	A
Total power dissipation		P_D ∗2	1.25	W / TOTAL
			0.9	W / ELEMENT
Channel temperature		Tch	150	℃
Range of Storage temperature		Tstg	−55 to +150	℃

∗1 Pw≤10μs, Duty cycle≤1%
∗2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth (ch-a)∗	100	°C / W / TOTAL
		139	°C / W / ELEMENT

∗ Mounted on a ceramic board

●**Electrical characteristics** (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2 MOS FET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±10V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–12	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –12V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–0.3	–	–1.0	V	V_{DS}= –6V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	75	105	mΩ	I_D= –2A, V_{GS}= –4.5V
		–	105	145	mΩ	I_D= –1A, V_{GS}= –2.5V
		–	150	225	mΩ	I_D= –1A, V_{GS}= –1.8V
		–	200	400	mΩ	I_D= –0.4A, V_{GS}= –1.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	2	–	–	S	V_{DS}= –6V, I_D= –2A
Input capacitance	C_{iss}	–	770	–	pF	V_{DS}= –6V
Output capacitance	C_{oss}	–	75	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	60	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	10	–	ns	V_{DD}≒ –6V I_D= –1A V_{GS}= –4.5V R_L≒6Ω R_G=10Ω
Rise time	t_r *	–	17	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	65	–	ns	
Fall time	t_f *	–	35	–	ns	
Total gate charge	Q_g *	–	6.5	–	nC	V_{DD}≒ –6V R_L≒3Ω I_D= –2A R_G=10Ω V_{GS}= –4.5V
Gate-source charge	Q_{gs} *	–	1.3	–	nC	
Gate-drain charge	Q_{gd} *	–	0.8	–	nC	

*Pulsed

●**Body diode** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	I_S= –2A, V_{GS}=0V

*Pulsed

●Electrical characteristic curves

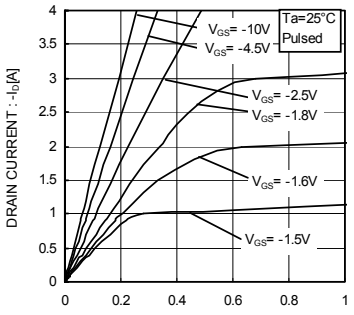


Fig.1 Typical Output Characteristics(Ⅰ)

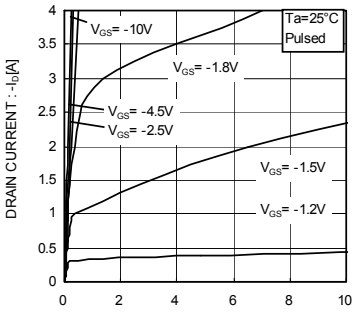


Fig.2 Typical Output Characteristics(Ⅱ)

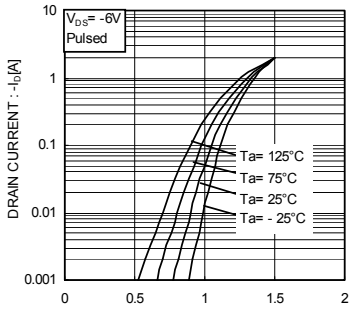


Fig.3 Typical Transfer Characteristics

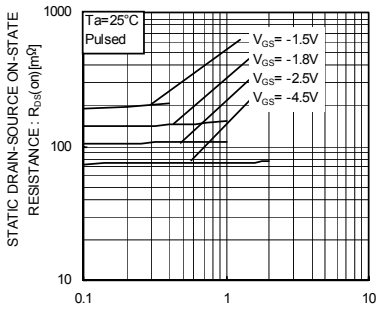


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

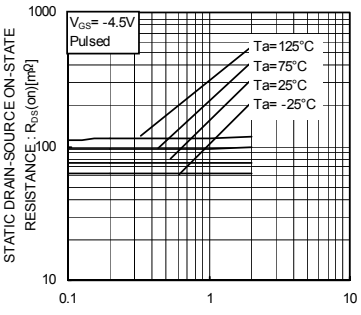


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

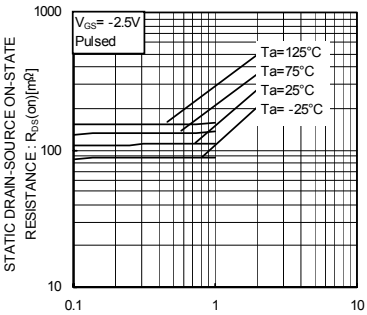


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

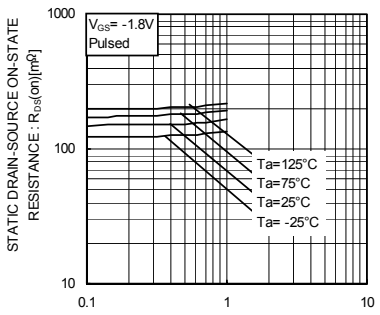


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

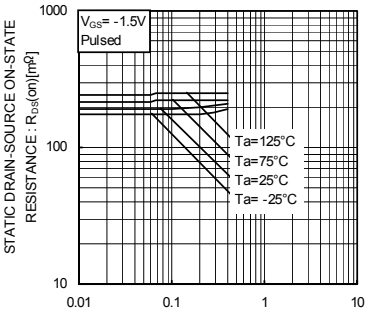


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅴ)

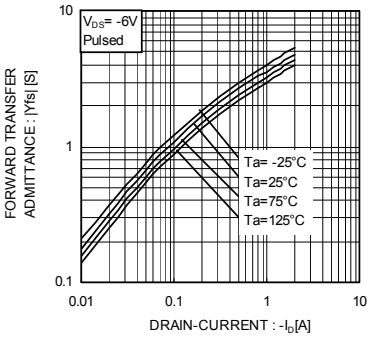


Fig.9 Forward Transfer Admittance vs. Drain Current

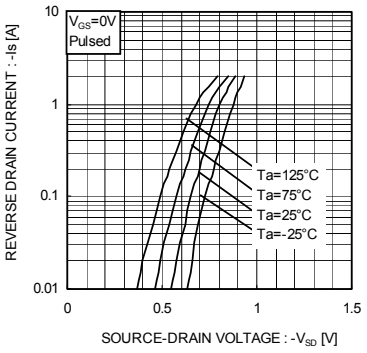


Fig.10 Reverse Drain Current vs. Sourse-Drain Voltage

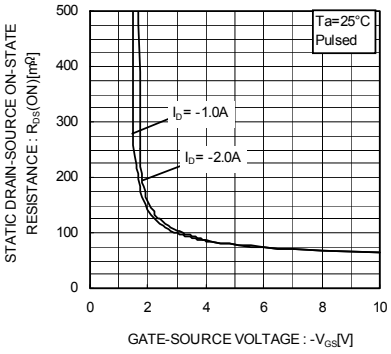


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

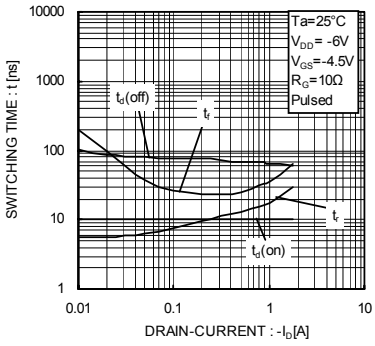


Fig.12 Switching Characteristics

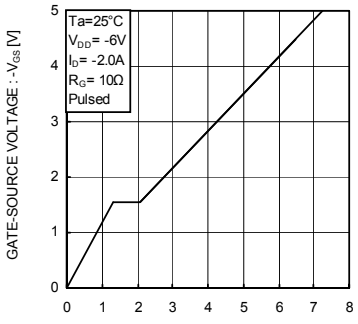


Fig.13 Dynamic Input Characteristics

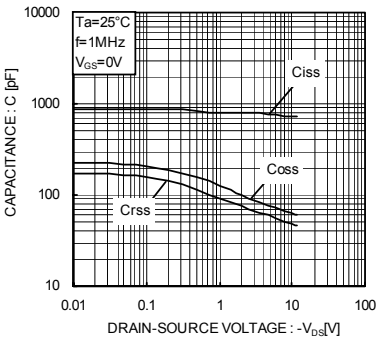


Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuits

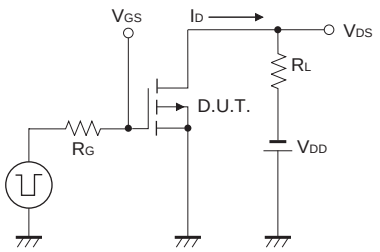


Fig.1-1 Switching Time Measurement Circuit

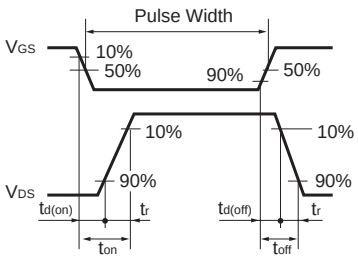


Fig.1-2 Switching Waveforms

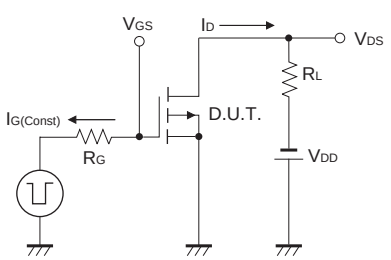


Fig.2-1 Gate Charge Measurement Circuit

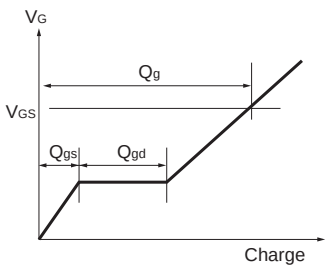


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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